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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,995	09/27/2001	Kazuo Ogawa	N29748500S	2991

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EXAMINER	
TRAN, THIEN F	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,995	OGAWA, KAZUO	
	Examiner	Art Unit	
	Thien F Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-7 and 9-25* is/are pending in the application.

4a) Of the above claim(s) *12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-7,9-11 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 22 is objected to because of the following informalities: line 4, "the inner walls" should be –inner walls—for lack of antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5-7, 9, 11, 21-23 and 25 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ishitsuka et al. (USPN 6,242,323).

Ishitsuka et al. discloses the claimed semiconductor device (Fig. 32) comprising a trench element separation region 4 including a trench 4a formed in a surface of a semiconductor substrate, the trench element separation region isolating separate semiconductor elements (isolating a first doped channel layer 14 of a first insulated gate field effect transistor from a second doped channel layer 15 of a second IGFET); an oxide film 5 (see Fig. 16) formed on inner walls of the trench to form a liner oxide film defined edged within the trench; a trench

filling insulating material 7 filling the trench and having (vertical) edges above the inner walls of the trench; and wherein inner wall edges in a top section of the trench and the edges of the trench filling insulating material 8 above the trench are formed so as to be essentially located on the same vertical plane when viewed in cross section.

The claim limitation reciting the edges of the trench filling insulating material being defined by direct contact with side edges of a sacrificial layer formed by a pull back etching process including a neutral radical performed before filling the trench (for the trench filling process) in claims 1 and 7; the limitation reciting the etching process including a fluorine radical in claim 9; and the limitation reciting neutral radical pullback etch in claims 22 and 25 are taken to be product by process limitations. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear. Claims 1, 7 and 22 clearly claim a final structure as depicted by Figure 2(c) in the application

wherein the trench element separation region separate semiconductor elements 12 and 14. As a result, the claim limitation reciting the edges of the trench filling insulating material being defined by direct contact with side edges of a sacrificial layer formed by a pull back etching process including a neutral radical performed before filling the trench (for the trench filling process) in claims 1 and 7 recite intermediate features in intermediate structures of Figures 1(c) - 1(d) of the application that no longer exist in the final structure (see Figure 2(c)). As far as device claims are concerned, the final structure as claimed "gleaned" from the process steps is not patentably distinguished over the structure of the prior art reference.

Regarding claim 3, the sacrificial layer is a silicon nitride film.

Regarding claim 5, the semiconductors elements are insulated gate field effect transistors (IGFETs).

Regarding claim 6, the IGFETs include opposite conductivity types.

Regarding claim 11, the first and second doped channel layers (14, 15) are of opposite conductivity types.

Regarding claim 21, Figures 15-16 and 20 of Ishitsuka show that above the surface of the substrate, the oxide film 5 extends essentially only horizontally and is formed below and terminates beyond the edges of the trench filling insulating material 7 above the inner walls of the trench.

Regarding claim 23, a diffusion layer 14 of the transistor is formed in the substrate adjacent to the trench.

Regarding claim 25, the liner oxide film 5 includes a substrate portion (see figures 15, 16), the substrate portion (a portion of oxide film 5) extending essentially only horizontally on a surface of the semiconductor substrate, formed below and terminating beyond the edge of the trench filling insulating material 7.

Claims 7, 9, 10 and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bhakta et al. (USPN 6,258,697).

Bhakta et al. discloses the claimed semiconductor device (Fig. 3G) comprising a trench element separation region including a trench 40 formed in a surface of a semiconductor substrate, the trench element separation region isolating a first doped channel layer 49 (a semiconductor element) of a first insulated gate field effect transistor from a second doped channel layer 49 (a semiconductor element) of a second IGFET; a liner oxide film 42 formed on inner walls of the trench to form a liner oxide film defined edge within the trench; a trench filling insulating material 46 filling the trench and having edges above the inner walls of the trench defined by side edges of a sacrificial layer 34 (Fig. 3E); and wherein inner wall edges in a top section of the trench and the edges of the trench filling insulating material above the trench are formed so as to be essentially located on the same plane when viewed in cross section.

The claim limitation reciting the edges of the trench filling insulating material being defined by direct contact with side edges of a sacrificial layer formed by a pull back etching process including a neutral radical performed before filling the trench in claim 7; the limitation reciting the etching process

including a fluorine radical in claim 9; and the limitation reciting a neutral radical pullback etch in claims 22 and 25 are taken to be product by process limitations. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear. Claim 7 clearly claims a final structure as depicted by Figure 2(c) in the application wherein the trench element separation region isolate a first doped channel layer 12 from a second doped channel layer 14. As a result, the claim limitation reciting the edges of the trench filling insulating material being defined by direct contact with side edges of a sacrificial layer formed by a pull back etching process including a neutral radical performed before filling the trench in claim 7 recite intermediate features in intermediate structures of Figures 1(c) - 1(d) of the application that no longer exist in the final structure (see Figure 2(c)). As far as device claims are concerned, the final structure as claimed "gleaned" from the process steps is not patentably distinguished over the structure of the prior art reference.

Regarding claim 10, the first and second doped channel layers 49 are doped at the same time. It is inherent that the first and second doped channel layers 49 are doped of the same conductivity type.

Regarding claim 23, a diffusion layer 49 is formed in the substrate adjacent to the trench.

Regarding claim 24, the liner oxide film 44 has a thickness of 10 - 20 nm which is greater than 7 nm.

Response to Arguments

Applicant's arguments with respect to claims 22-25 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 06/17/2004 have been fully considered but they are not persuasive. Applicant argues about the differences between the processes in the application and the prior art references and thus the structure as claimed is different from the structures as described in the prior art references. However, it is the examiner's position that the presence of process limitations in product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephens 145 USPQ 656 (CCPA 1965). In a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or slightly different than the product claimed in a product-by-process claim, a rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it

and then obtain prior art product and make physical comparisons therewith. In re Brown, 173 USPQ 685 (CCPA 1972).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tt
August 26, 2004

THIEN TRAN
PRIMARY EXAMINER